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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,705	03/19/2004	Yu-Ling Chiu	ALIP0042USA	2704
27765	7590	05/17/2005	EXAMINER	
NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)			OWENS, DOUGLAS W	
P.O. BOX 506			ART UNIT	
MERRIFIELD, VA 22116			PAPER NUMBER	
			2811	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/708,705

Applicant(s)

CHIU ET AL.

Examiner

Douglas W. Owens

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 22 February 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1 – 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 requires that the solder pad separate the first bonding line from other bonding lines. The scope of the claim is nebulous, since it is not known how a solder pad can be used to isolate lines one from another.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,417,532 to Tsunoda et al. in view of US Patent No. 4,513,355 to Schroeder et al.

Regarding claims 1 and 9, as far as an indefinite claim can be understood, Tsunoda et al. teach a wire bonding package (Fig. 16) comprising:

a housing (94) having a plurality of pins (95) installed;

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a circuit board (92) installed inside the housing, the circuit board comprising at least a trace connected to the pins of the housing;

at least a die (91) installed on the circuit board, the die having a plurality of bonding pads installed;

and at least a bonding line connected between the bonding pads of the die and the trace of the circuit board so that the bonding pads of the die are electrically connected to the pins of the housing (Col. 1, lines 30 – 41).

Tsunoda et al. do not teach a package further including a solder pad soldered to the first bonding line at a point on the first bonding line between the bonding pad of the die and the trace of the circuit board for separating the first bonding line from other bonding lines, wherein the solder pad is located on the circuit board. Schroeder et al. teach that it is common to attach a bonding line with a soldered connection (Col. 2, lines 22 – 27). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Schroeder et al. into the device taught by Tsunoda et al. and attach the line with solder to the circuit board, since it is desirable to provide strong reliable connections for bonding lines.

Regarding claim 4, Tsunoda et al. teach a package, comprising a plurality of die, at least two of the die adhering to the circuit board.

5. Claims 1, 2, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2004/0118587 to Gilliland in view of Schroeder et al.

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Regarding claims 1 and 9, as far as an indefinite claim can be understood, Gilliland teaches a wire bonding package (Fig. 1) comprising:

- a housing (14) having a plurality of pins installed;
- a circuit board (30) installed inside the housing, the circuit board comprising at least a trace connected to the pins of the housing;
- at least a die (28) installed on the circuit board, the die having a plurality of bonding pads installed;
- and at least a bonding line (42) connected between the bonding pads of the die and the trace of the circuit board so that the bonding pads of the die are electrically connected to the pins of the housing.

Gilliland does not teach a package further including a solder pad soldered to the first bonding line at a point on the first bonding line between the bonding pad of the die and the trace of the circuit board for separating the first bonding line from other bonding lines. Schroeder et al. teach that it is common to attach a bonding line with a soldered connection (Col. 2, lines 22 – 27). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Schroeder et al. into the device taught by Gilliland and attach the line with solder to the circuit board, since it is desirable to provide strong reliable connections for bonding lines.

Regarding claim 2, Gilliland teaches a package, wherein the housing comprises a lead frame (44) for accommodating the circuit board.

Regarding claim 8, Gilliland teaches a package further comprising at least a passive component (28) installed on the circuit board (paragraph [0036]).

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6. Claims 3 and 5 – 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilliland and Schroeder et al. as applied to claim 1 above, and further in view of US Patent No. 6,744,126 to Chiang.

Regarding claim 3, the proposed device of Gilliland and Schroeder et al. do not teach a plurality of die stacked on a circuit board. Chiang teaches a stacked chip arrangement (Col. 3, lines 1 – 21). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Schroeder et al. into the proposed device of Gilliland and Schroeder et al., since it is desirable to reduce the size of the package.

Regarding claims 5 – 7, Gilliland and Schroeder et al. do not teach a package that can be a BGA, QFP or DIP. Chiang teaches a package, wherein the housing can be configured in BGA, QFP or DIP arrangements (Col. 24, lines 46 – 60). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Chiang into the proposed package of Gilliland and Schroeder et al., since it is desirable to accommodate a plurality of design specifications.

7. Claims 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,417,532 to Tsunoda et al. in view of US Patent Application Publication No. 2003/0151133 to Kinayman et al.

Regarding claim 10, Tsunoda et al. teach a wire bonding package (Fig. 16) comprising:

a housing (94) having a plurality of pins (95) installed;

a circuit board (92) installed inside the housing, the circuit board comprising at least a trace connected to the pins of the housing;

at least a die (91) installed on the circuit board, the die having a plurality of bonding pads installed;

and at least a bonding line connected between the bonding pads of the die and the race of the circuit board so that the bonding pads of the die are electrically connected to the pins of the housing (Col. 1, lines 30 – 41).

Tsunoda et al. do not teach a first and second via formed in the circuit board, the first bonding line passing through the first and second vias such that a section of the first bonding line between the first and second vias is located beneath the circuit board. Kinayman et al. teach a first and second via formed in the circuit board, the first bonding line passing through the first and second vias such that a section of the first bonding line between the first and second vias is located beneath the circuit board (Fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Kinayman et al. into the package taught by Tsunoda et al., since it is desirable to provide a versatile connection.

Regarding claim 13, Tsunoda et al. teach a package, comprising a plurality of die, at least two of the die adhering to the circuit board.

Claims 10, 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2004/0118587 to Gilliland in view of Schroeder et al.

Regarding claim 10, Gilliland teaches a wire bonding package (Fig. 1) comprising:

a housing (14) having a plurality of pins installed;

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a circuit board (30) installed inside the housing, the circuit board comprising at least a trace connected to the pins of the housing;

at least a die (28) installed on the circuit board, the die having a plurality of bonding pads installed;

and at least a bonding line (42) connected between the bonding pads of the die and the trace of the circuit board so that the bonding pads of the die are electrically connected to the pins of the housing.

Gilliland does not teach a first and second via formed in the circuit board, the first bonding line passing through the first and second vias such that a section of the first bonding line between the first and second vias is located beneath the circuit board.

Kinayman et al. teach a first and second via formed in the circuit board, the first bonding line passing through the first and second vias such that a section of the first bonding line between the first and second vias is located beneath the circuit board (Fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Kinayman et al. into the package taught by Gilliland, since it is desirable to provide a versatile connection.

Regarding claim 11, Gilliland teaches a package, wherein the housing comprises a lead frame (44) for accommodating the circuit board.

Regarding claim 17, Gilliland teaches a package further comprising at least a passive component (28) installed on the circuit board (paragraph [0036]).

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Claims 12 and 14 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilliland and Kinayman et al. as applied to claim 10 above, and further in view of US Patent No. 6,744,126 to Chiang.

Regarding claim 12, the proposed device of Gilliland and Kinayman et al. do not teach a plurality of die stacked on a circuit board. Chiang teaches a stacked chip arrangement (Col. 3, lines 1 – 21). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Kinayman et al. into the proposed device of Gilliland and Kinayman et al., since it is desirable to reduce the size of the package.

Regarding claims 14 – 16, Gilliland and Kinayman et al. do not teach a package that can be a BGA, QFP or DIP. Chiang teaches a package, wherein the housing can be configured in BGA, QFP or DIP arrangements (Col. 24, lines 46 – 60). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Chiang into the proposed package of Gilliland and Kinayman et al., since it is desirable to accommodate a plurality of design specifications.

### ***Response to Arguments***

8. Applicant's arguments with respect to claims 1 – 17 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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A handwritten signature in black ink, appearing to read "Douglas W Owens". The signature is written in a cursive, flowing style.

Douglas W Owens  
Examiner  
Art Unit 2811

DWO